Hello Yair
Here is the outcome of my action item to ponder rows 4 & 5 in the table that was being discussed during ad hoc meeting #3:

I was reviewing the version 2.5 draft, and discover this text at the beginning of clause 145.5.3.3:

"This subclause contains the variables and state diagrams the PSE uses when connected to a single-signature PD, or when it is providing power over 2 pairs."
Yair: Correct.

Single signature AND 2 pair powering topologies should only use the 'Y' field as defined in your table.
Yair: Meantime, we all agree that it should use Y field. The issue under discussion per my proposal is if we need to use also A field or B field while A or B is the active field. The non-active field in my proposal is set to zero.

There is no need for the additional complexity of a case where 'Y', 'A', and 'B' are all set to non-zero values. (I have a great deal of difficulty accepting the direction that the 'solution' is going in that requires defining a non-zero value for the mode that is NOT being powered.)
Yair: John, you got it wrong OR you have a typo in your statement above. Please let me know what it is.
-I am not saying "where 'Y', 'A', and 'B' are all set to non-zero values" I am saying just Y and (A or B) are set to non zero.
-I am not saying that "the 'solution' is going in that requires defining a non-zero value for the mode that is NOT being powered.)". I am saying that a non-zero value will set for the active mode and a zero will set in the non-active mode. Please check again the table and let me know if you have a typo or it is something else.

If you can accept the premise that the Dual Signature PD power control state diagram is only relevant when a Dual Signature PD is being furnished power over 4 pairs, then the cases that need to be addressed can be reduced to those that are already described in the draft.
Yair: I can accept this premise but I am not sure that the current draft will not need to be changed due to other issues.

Rows 4 & 5 in the table (labelled as "Part of Figure 79-3")
Yair: Not sure what you meant in this statement? Did you meant that rows 4 and 5 are covered by Figure 79-3? If YES then I agree.

With respect to the Dual Signature PD power control state diagram, when power is being provided over 2 pairs, the relationship between 'Y' (requested or allocated power) and the active mode ('A' or 'B', never both) is being defined in a manner that is adding substantial (and I argue unnecessary) complexity.
Yair: "substantial complexity". I totally disagree. The complexity is equivalent to X➔Y or 1+1=2 as simple as that.
Regarding "unnecessary" you may be correct and this is what I am looking for to verify.

The table as of the completion of ad hoc meeting #3 contains the proposed change defines that Y=Alt(X) for the PSE and Y=mode(X) for the PD

Yair: I hope that you argue only about the need for Y=ALT(X) and not about Y=Mode(X) since for the PD you must have it otherwise the state machine will not work and you have to have A and B in the PD regardless if it 2P or 4P. **LENNART please address this issue as well. We both analyze it and agree that in the PD it is required. The doubts are only in the PSE.**

That correctly describes the relationship of the power Y for the single active mode. Consider the following argument regarding why Alt(X) and mode(X) are irrelevent for the 2 pair powering case:

The statement in 145.5.3.3 already defines that the PSE will use the state diagram in Figure 145-40 when powering over 2 pairs.

Yair: Correct.

A Type 3, class 4 PD already has a need to conceptually implement the Single Signature PD power control state diagram when connected to a Type 2 PSE that only implements the 12 octet Power via MDI TLV (per clause 79, 802.3-2015), since the 'Y' field is the only one that will exist. The same is true for Type 3, class 1, 2, and 3 PDs (which support LLDP) connected to a Type 2 PSE, or Type 1 PSE that implements LLDP (there are some of these in existence).

Yair: Correct.

This same concept would directly address the PD end of the power negotiation when the DS PD is only being furnished power over 2 pairs by a Type 3 or 4 PSE, or a Type 1 or 2 that has been updated to use the new extended Power via MDI TLV.

Yair: I agree from consistency point of view.

If a statement similar to the one in clause 145.5.3.3, for example:

" This subclause contains the variables and state diagrams the PD uses when connected to a PSE that is providing power over 2 pairs."

were added to 145.5.3.4, there would be no need for the Dual Signature PSE power control state diagram to be modified.

Yair: I agree to add it.

A similar statement, such as:

"This subclause contains the variables and state diagrams the Dual Signature PD uses when connected to a PSE that is providing power over 4 pairs."

would need to be added to 145.5.3.7,

Yair: I agree to add it.

and something like this to 14.5.3.6:

"This subclause contains the variables and state diagrams the PSE uses when connected to a dual-signature PD, when it is providing power over 4 pairs."

Yair: I agree to add it.

Note that one of the topics that has been discussed during the ad hoc is the concept of a possible transition from 4 pair to 2 pair, or 2 pair to 4 pair powering. There does not appear to be any discussion of how such a transition would be accomplished in either text or the DLL state diagrams.

Yair: We agree to add text to explain it but not to change the DLL state machine.

I would anticipate that this would need to be coupled to a change in the PSE power pairsx bits in the Power status field. When PSE power pairsx indicates "Both Alternatives" and Power classx

indicates "Dual-signature PD", the mode(X) power fields would be used, and the PSE and PD would need to be in sync as defined in 145.5.5. When PSE power pairsx indicates "Alternative A" or "Alternative B", then the sync rules as defined in 145.5.4 would apply. If such a transition is to be supported, and devices are expected to be able to interoperate, then the spec will need to define this.
Yair: Obviously we want to support this transition from 4-pairs to 2-pairs and back. It is supported in the physical layers state machines. So it need to be supported in the DLL state machine. We don't need to change DLL state machine, we need just to add text to explain this. Regarding Power classX etc. Please let us know what you are proposing to change or clarify in a baseline format so we can review it.